ISSN:2320-0790

An International Journal of Advanced Computer Technology

Low latency on chip communication based on hybrid NOC Architecture using X-Y router

Tejaswini Deotare[1], P.R.Rothe[2]
[1]M Tech 4th sem VLSI, PCE, RTM Nagpur University, Nagpur, India
[2]Dept. EE, PCE, RTM Nagpur University, Nagpur, India

Abstract- On-chip communication has two different type of architecture which can be classified as Bus and mesh based Networks-on-Chip (NoC). Each of them has different features and applications. In this paper, we construct the hybrid architecture with using bus and mesh NOC architecture. In the hybrid architecture, heavy communication affinity IP cores are placed in the same subsystem. and this large mesh NoC get partitioned into several subsystems and one on one individual IPs, so that there is the reduction in the transmission latency of NoC . Efficient partition and mapping algorithm is proposed for reduction of the latency on the hybrid NOC architecture. It shows that an average latency improvement of 17.6% and more can be obtained when compared with the conventional mesh NoC architecture.

Keywords— Hybrid NOC architecture, x-y Routers, IP cores, mesh architecture

I. INTRODUCTION

Semiconductor technology have been increased very fastly and there is rapid advanced in the technology. When it comes to the semiconductor technology it consist of IP core that is functional Intellectual property (IP) and it is placed on single chip .All this IP are placed in single chip. Complex bus system which is developed by using the connection that is connecting all IP for the development of modern SOC design. Unfortunately, there is a limitation of scalability in the bus based communication. If the IP core is increased communication performed is also decreases. This bus architecture has to be solved for future SOC and many paper has been proposed.(network-on-chip) NOC is one of them. NoC systems maps the IP on a block and transmit data between the IP using network communication.

In this paper, we propose bus-mesh hybrid architecture for SOC design which provides a communication of the data having low latency. IP can decide the location each of them. The idea is to extract is to extract the communication feature of the IP which decide their location. In the proposed hybrid architecture IP are placed in the same sub system which has a high communication affinity and have high data traffic. which help in the reduction in the hot-spot and reduce the transmission latency. Truly, the hybrid architecture is based on the NOC concept, the router which is used to connect the system also connect to the neighboring routers but also connect to the single IP or a bus based subsystem. Design interface is not needed for each IP, which can further reduce the design cost and power consumption also.

As there is the increase in the fabrication in the semiconductor technology which continues to improves in the small size and allows to integrate the more system components on the single die.If the carefull attention is not given on the designing high performance interconnect the communication between this component becomes the limited factor. This project implements an on-chip SoC interconnect embodying the X-Y router and i-SLIP scheduling algorithm for efficient communication between SoC devices. It provides fast communication and full N-to-N routing capabilities. But efficiently we will focus on the X-Y router, which will help in reduction in the low latency on chip communication.

The design challenges are discussed in section II, followed by proposed work in section III, and the related work is visited in section IV.

II. DESIGN CHALLENGES

In the existing system, the Hybrid NOC architecture is used. The hybrid system consist of the several bus based subsystem and its based on NOC architecture. Heavy traffic load IP are placed in same subsystem. The figure shows the Hybrid NOC architecture, it is shown in the fig 1 .R denotes the router, S denotes the sub system, C denotes the single IP core, B denotes the bridge of NOC and bus. These are the important components. Every subsystem consist of certain architecture.NOC and Bus architecture is interface by the the bridge. If the data transfer takes place from subsystem to network, bridge can be serves as the slave components of the bus and which is used to receives the control data vfsignals, addresses from the master components. Bridge helps to packetize them into packets and delivered the packet to router. Next condition is anises from the ,when data is transfers from network to subsystem ,bridge serves as

the master components and depacketized the packet ,then send all the data to the corresponding IPs.

The hybrid system consists of bus and NoC architecture. the latency models of bus and NoC architecture is calculated by the formulas. There are some problems which is also given in the further section. Further section of the paper gives section a gives the formula for the calculation of the bus latency .while the section B gives the formula for the Noc latency. Section C discussed some of the few problems.

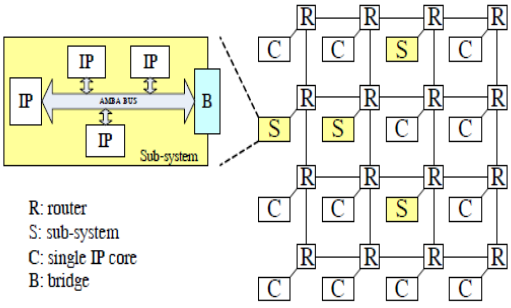


Fig. 1. Hybrid NoC architecture

A. BUS LATENCY FORMULA:

This section will show the formula for the calculation of the latency of the bus with the single master.

$$L_{bus} = (3-2U)\cdot N_D \cdot S + \lceil \frac{N_D \cdot (1-S)}{B} + N_D(1-S) \rceil$$

Where ND is the number of data, S is the rate of single mode transfer, B is the size of burst data and U is the usage of bus.

But with more bus masters rather than one then it is given by the next formula given below.

$$L_{single\_layer} = N_M \cdot L_{bus}$$

B. NOC LATENCY FORMULA:

This section will show the formula for the calculation of the latency of the NOC. The packet transmission latency in NoC includes the delay of router and network interface.

$$L_{NoC} = n \times L_{router} + m \times L_{NI}$$

Where L router is the transmission latency of a router to transmit a fixed size packet, the LNI is the latency of network interface to encode or decode a packet. n and m denote the number of routers and number of network interfaces.

PROBLEM DESCRIPTION:

For different applications, the bandwidth requirements are also different. To define the hybrid NoC problem, the bandwidth requirement of a system is represented as a communication graph.

The communication graph is a directed graph to solve the problem we have to decide the problem associated. In the problem, we try to decide which IP should be assigned to the same subsystem and which maps the subsystems on to the Hybrid system such that the total communication cost is minimized under bandwidth constrain.this proposed work can be done using VHDL or VERILOG. This is done in the proposed paper using VHDL,using modelsim software.

III. PROPOSED WORK

This paper proposed a system which consists of the mesh having a four by four matrix. Here to pass the data the routers are used. The implementation of the hydrid architecture the data is passed to two different meshes. The two matrix of the same order is been programmed and the first matrix is made and data is passed through X-Y router .The X-Y router is used to reduce the latency as compared to other router algorithm .X-Y router algorithm is used so that the data is passed in very fast manner and the hardware implementation is also required less as compare to the other routers.

In the X-Y routers the name implies that the data is passed either in X direction or in Y direction .data is not passed digonally in in the matrixs .the way of processing of the data in the matrixs in the X-Y router is such that it will not provide any delay as other algorithm .ther data passing algorithm is use the delay occurred in choosing the path ,while in X-Y router chose the path instantly without any delay and low latency communication is occurred .The matrix that can be changed but in this proposed architecture the four by four matrix is consider. the specific logic is allotted for the passage of the data in the mesh matrix .It consist of the 16 bit data consist of 0 to 15 bit where it consist of the specific order and data which is going to pass through the mesh. The detail of the 16 bit is described below. This 16 bit that is the order of the bit is called as the frame format of the X-Y router.

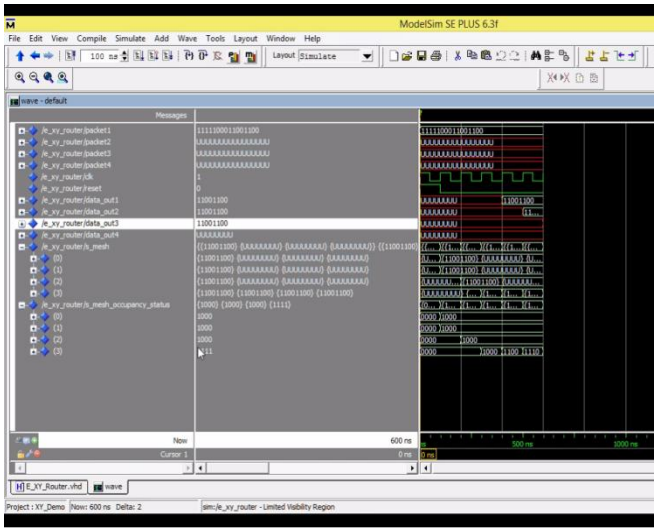
If we consider the mesh having the four terminal inputs. These four terminals is name as R1, R2, R3, R4. And the four by four matrix are such that the first row contains the matrixs having the address 0,0; 1,0; 2,0; 3,0; likewise second row contains the second matrix havin 0,1; 1,1; 2,1; 3,1; for third row contains the order 0,2; 1,2; 2,2; 3,2; fourth row consist of the order 0,3; 1,3; 2,3; 3,3; .Here consider the 0,1 matrix it means that address of the destination x address is 0, and address of the destination Y address is 1. The data will pass either in X direction or in Y direction .The direction is specified by the address of the block. There is the frame formate which will give the proper way to pass the data.

In the Frame format from bit 0 to 7 that is of 8 bit consist of data that has to be passed .From bit number 8 to 10 that is of 3 bit is taken as the don't care bit can be treated as the either 0 or the 1. The 11 and 12 bit of the frame format is consisting o f the address of the y matrix. The 13 and the 14 bit consit of the x matrix address. the 15 bit is that bit which gives the address of the input terminal from where the input is passed . That is from R1, R2, R3, R4. This 15 bit is made enable by making it as 1.

Consider the following example; we made the programming of the four by four matrix and we want to pass the data from the matrix 0, 0 to 3, 3 using X-Y routher. The input should Be from first terminal R1.Data passed is given as 1100 1100 that is from 0 to 7 bit. Frame format will be 1111100011001100. Here the r1 terminal is selected as the input so 15 bit is enable that is 1, destination address x,y is 3,3 so bit from 14 to 11 is 1111. 10 to 8 bit is treated as 000 ,and from bit 0 to 7 is the data .Data to be passed is 1100 1100.the following output will be shown in the printscreen.at clock is 1 and reset is 0 then the data is passed to 3,3 matrixs. Then passage of data in the matrix form is shown in the output.

IV. RELATED WORK

Since in the hybrid NOC architecture data is passed from one mesh terminal to another end of mesh terminal here by using X-Y router .In the data communication it is observed that the latency of the data communication has been less as compared to the other proposed algorithm . Another work is proposed by using i-slip algorithm which is another mesh algorithm form to pass the data though the mesh matrix and the latency of the communication is measured .Overall give the less latency. The proposed work gets compared with the normal as well as the other router algorithm to measure the latency of the data communication. The following image shows the output of the proposed work.



V. CONCLUSION

The proposed work in the hybrid NOC architecture help use to reduced the latency of the data communication, the hardware requirement is also less and the bandwidth requirement is also less.

Here the IPs are been attached with the bus for the data traffics.Here the IPs are been mapped on the hybrid system under the bandwith constraint and its placed such that the average communication latency .For the unbalned communication requirement this architecture is suitable.

VI. REFRENCES

[1] S. Bourduas and Z. Zilic, "A hybrid ring/mesh interconnect for networkon chip using hierarchical rings for global routing," in *International Symposium on Network-on-Chip*, 2007, pp. 195–204.

[2] H. M. Harmanani and R. Farah, "A method for efficient mapping and reliable routing for noc architectures with minimum bandwidth and area," in *IEEE Northeast Workshop on Circuits and Systems and TAISA Conference*, June 2008, pp. 29–32.

[3] W. Lee and G. E. Sobelman, "Mesh-star hybrid noc architecture with cdma switch," in *IEEE Proc. of International Symposium on Circuits and Systems*, 2009, pp. 1349–1352.

[4] T. D. Richardson, C. Nicopoulos, D. P. andV. Narayanan, Y. Xie, C. Das, and V. Degalahal, "A hybrid soc interconnect with dynamic tdma-based transaction-less buses and on-chip networks," in *Proc. of International Conference on VLSI Design*, 2006.

[5] Y. S. Cho, E. J. Choi, and K. R. Cho, "Modeling and analysis of the system bus latency on the soc platform," in *Proc. of International workshop on System-Level Interconnect Prediction*, 2006, pp. 67–74.

[6] J. D. Wang, "Low power mapping of cores onto hybrid noc architecture," Master's thesis, National Taiwan University, 2007.

[7] Wijetunga, P., "High-performance crossbar design for system-on-chip," *System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE International Workshop on* , vol., no.pp. 138- 143, 30 June-2 July 2003.

[8] Pape, J; "Implementation of an On-chip Interconnect Using the i-SLIP Scheduling Algorithm: Intermediate Report – Specification and Timeline," Nov 2006.

[9] Mhamdi, L., Kachris, C., and Vassiliadis, S. 2006. A reconfigurable hardware based embedded scheduler for buffered crossbar switches. In *Proceedings of the 2006 ACM/SIGDA 14th international Symposium on Field Programmable Gate Arrays* (Monterey, California, USA, February 22 - 24, 2006). FPGA '06. ACM Press, New York, NY, 143-149.