EXPERIMENTAL INVESTIGATION OF SVM SWITCHING CONTROLLER BASED TWO-LEVEL VOLTAGE SOURCE INVERTER FOR PHOTOVOLTAIC SYSTEM USING DSP-TMS320F28335

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Abstract: Many switching schemes can be utilized to control the voltage source inverter (VSI). The harmonic appears at the VSI output waveforms using any control schemes. The space vector modulation (SVM) seems to be more effective than the other switching schemes. Therefore, this paper presents an experimental investigation of SVM switching controller based two-level voltage source inverter (VSI) for photovoltaic system. The robustness of the proposed SVM is investigated with a hardware that is implemented via a DSP-TMS320F28335 controller. The experimental investigation is accomplished for the SVM in terms of total harmonic distortion (THD). Two types of loads are utilized which are resistive (R) load and resistive and inductive (RL) load to investigate the performance of the SVM. The results of the proposed SVM are compared with sinusoidal pulse width modulation (SPWM). The implementation of the SVM via a DSP-TMS320F28335 controller is verified in the laboratory using a prototype two-level SVI. The THDs based SVM are found to be 2.0% and 2.6% for the R and RL, respectively; whereas the THD based SPWM are found to be 2.2% and 3.1% for the R and RL, respectively. This indicates that high quality waveforms with low THD have been obtained with SVM.

Keywords: Space vector modulation (SVM); Two-level voltage source inverter; Photovoltaic (PV); DSP-TMS320F28335

1. Introduction

Renewable energy resource (RER) is one of the most important sources of energy at the present time; it is widely used as a result of the negative effect of energy fuel (fossil fuels). The RER have turned into the significant rationale of the vitality division since they are free, clean, and ecological cordial [1]. Fuel cell, wind turbine, and photovoltaic system (PVS) are considered as RER. The RER are viewed as huge on the grounds that they have vital advantages, for example, for all intents and purposes accessible around the world, following vast vitality supply, and pollutions-free maneuver [2].

One of the most extensive uses of renewable energies is PVS. Where, the PVS is by all accounts the most significant part because of colossal accessibility of the sun powered where the earth got the sunlight based from the sun ten times the aggregate vitality spend by the entire world amid a year [3]. Moreover, the PVS can be utilized as a part of rustic regions and industrial power system as a result to get rid of the pollution problems that accompany the others types of energy provider. In any case, the process of converting solar energy into electrical energy needs to electronic circuit known as the voltage source inverter (VSI), where the VSI is imperative to interface the PVS to the load for producing the DC power. The VSI must have the capacity to supply brilliant waveforms with regards to a standalone PVS. The VSI can be controlled by numerous ways; every way creates some distortion at the VSI waveforms [4].

Around of the force quality issues are voltage plunges, clamor, voltage gleams, and harmonics. The harmonic is by all accounts the principle power quality issue [5]. Harmonic leads to gear overheating, expanding of misfortunes, and waveforms bending [6]. Therefore, total harmonic distortion (THD) measures the output waveform value of the harmonic level of the system. THD is profoundly relies on the pulse width modulation (PWM) switching scheme. Along these lines, the VSI execution can be refined

by applying an appropriate PWM switching scheme. Various PWM schemes have been reported in the literature, for example carrier based pulse width modulation, third harmonic injection pulse width modulation, sinusoidal pulse width modulation, and space vector modulation. However, PWM switching techniques utilized are sinusoidal pulse width modulation (SPWM) and space vector modulation (SVM).

Numerous controllers have been utilized to implement the switching controller including field-programmable gate array (FPGA), dSPACE and digital signal processing (DSP) controllers. In [7], the FPGA was used to implement reflex charge control with maximum power point tracking. In this study, the optimum gain of the PI controller was obtained using particle swarm optimization method. Ghani et al. was developed a simulation model linked prototype development of a PV inverter using the dSPACE DS1104 board based SPWM [8]. The proportional integral (PI) controller has been used to create the switching signals to the insulated-gate bipolar transistor (IGBT) switching exchanging, in this way producing the 50 Hz sinusoidal AC waveforms. In [9], the optimum fuzzy logic photovoltaic inverter controller was implemented using DSP control board. Given that both techniques, SPWM and SVM, are suggested, hence, this study is directed to assess the execution of the VSI based SPWM and SVM procedures.

In the present study, execution assessment of the SPWM and SVM switching controller based two-level photovoltaic voltage source inverter is proposed. This paper involves six sections. Section 2 portrays the concepts of the voltage source inverter; nature-inspired optimization based voltage controller has been introduced in section 3. The real-time implementation of the SPWM has been drawn in section 4; the real-time implementation of the SVM has been portrayed in section 5. The results have been examined in section 6. Finally, the conclusion has been written in section 7.

2. Concepts of the voltage source inverter

The processes of power conversation lead to power quality problems, where the inverter power quality is the import criterion of power quality. Hence, the waveform of the VSI output must acquire low THD level. However, the electromagnetic phenomenon which depicts the voltage or current in a specific time is alluding to "power quality" (PQ) term [10,11]. In addition, Breakdowns loads and abnormal working leads to a decrease or absence of power quality. Therefore, more of researches concentrate on using RES due to high power quality comparing with other systems to preserve good PQ for the reliable work of loads. Along these lines, numerous PQ standards are suggested, for example, IEC61727, IEEE1547, IEEE 929-2000, and EN61000-3-2 [12-14].

Moreover, the voltage and current components are called the harmonic distortions (HD) which perform multiples of the fundamental frequency. Where, the HD is the changing in the original voltage or current waveforms because of the presence of harmonics. Numerous issues can be happen because of the presence of harmonics, for example, decreased power factor, malfunction of sensitive equipment, and premature failure of transformers. So, the THD is using to compute the rate of the HD in an electrical power system. Therefore, the THD is the rate of all harmonic components of the voltage components to the voltage magnitude of the fundamental frequency [15].

Furthermore, another important issue of the power quality system is the maintain stability. Hence, a suitable control design must be implement whether the system connect as a grid-connected or as a stand-alone. Two control plans have been discovered relies on upon the connected modes which are current control design and voltage control design. The current control design is typically utilized in grid connected mode; in the meantime voltage control design is utilized as a part of stand-alone mode.

In current control mode, the point is to direct the current that the inverter supplies into the system [5]. In voltage control mode, it is important that the inverter creates an appropriate voltage waveform where the voltage must be kept with altered amplitude and frequency [16]. Since the PV voltage source inverter is proposed for stand-alone system, hence the voltage control mode is proposed in this work as will be written in the following sections.

3. Nature-inspired optimization based voltage controller

The prime example for the voltage controller for PV remains solitary VSI is portrayed in Fig. 1. It is comprise from PVS, VSI, LC filter, voltage controller, and switching signal technique. The financially accessibility is the primary driving force of the using for the IGBT in this study. The proposed voltage controller created in this study is premise of two FLC controllers.
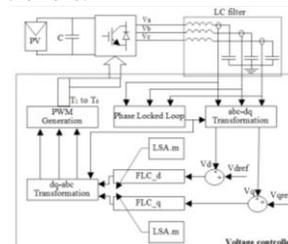

Fig.1. The Block diagram of the proposed voltage controller for the VSI.

The implementation of FLC is required three steps which are fuzzification, inference engine design, and defuzzification [17]. The time-consuming trial-and-error procedure used to tune membership functions (MFs) limits in the fuzzification step is the primary shortcoming of FLC configuration. The poor performance in the system is possibly because of wrong determination of MFs limits Therefore, nature-inspired optimization known as lightning search algorithm (LSA) has been used to decide the MFs limits which is begins by resetting the number of iterations (T), dimension of the problem (D), step leader size (N), and channel time. More insights about LSA usage to decide the limit estimations of membership functions MFs can be found in [4].

The evaluation performance of two-level VSI has been achieved by using two types of switching controller. The first switching controller technique is the SPWM; in the meantime the second switching technique controller is the SVM which are the most vital switching controller types. The following two segments will depict the advancement of these two switching controller techniques.

4. Real-time implementation of the SPWM

SPWM is an important method used to generate and transfer switching signals to the IGBTs and thus produce the AC output voltage close to the sine waveform as possible [18].The modulating signal in the SPWM is compared with the carrier signal to produce the PWM signals for the power devices. In this study, the modulating signal is 50 Hz, and the carrier signal is 5 kHz. The frequency of the triangular carrier signal creates inverter switching frequency, at which power devices, such as IGBTs, is switched. The PWM signals are created by comparing a sinusoidal reference signal (desired waveform) with a triangular carrier of frequency, *fc*, that establishes a switching frequency [19]. With the PWM method, the VSI can achieve a sinusoidal output waveform [20].

The SPWM technique is implemented in real-time using a DSP-TMS320F28335 controller (Fig. 2). The real-time model implementation via the DSP-TMS320F28335 controller includes a C280x/C28x3x analog-to-digital converter (ADC) and a C280x/C28x2833x enhanced PWM (ePWM). The first block in the real-time model is the ADC, which is used to sample the VSI output voltages (V_a, V_b, and V_c). The outputs from the voltage sensors are fed to pins 2, 3, and 4 from port 5 (ADCINB1, ADCINB2, and ADCINB3). The ADC input varies from 0 V to 3 V, and the output is varying from 0 to 4095 because the ADC is 12 bits. The ADC output can be defined as:

$$ADC_{output} = \begin{cases} 0 & ADC_{input} \leq 0\,V \\ 4096 \times \frac{ADC_{input}}{3} & 0\,V < ADC_{input} < 3\,V \\ 4095 & ADC_{input} \geq 3\,V \end{cases}$$

(1)

The output from the ADC (ADC_{output}) should be subtracted from the bias, half of the highest value, to generate the actual signal. The value of 1535 is approximately half of the highest value.

The most important blocks in the real-time model implementation via a DSP-TMS320F28335 control board are C280x/C28x2833x ePWM blocks. Three ePWM blocks are used (Fig. 2). The ePWM blocks are responsible to generate the switching signals to the IGBTs. An important factor that needs to be considered in designing experimental PWM switching is the dead time, which is the time delay between the upper switch (e.g., IGBT1) turning ON time and the lower switch (e.g., IGBT4) turning OFF time. The operation of both IGBTs at the same leg leads to the shoot-through phenomenon, where the DC input source may become short circuited. This phenomenon causes large current flow through the IGBTs and damages not only the devices, but also the unprotected input source. The amount of delay between the upper and lower switches is programmed using the dead-band rising-edge (D_{RED}) and dead-band falling-edge (D_{FED}) registers. Given that D_{RED} and D_{FED} are 10 bits, these parameters can be set to values from 0 to 1023. The delay for the rising and the falling can be calculated as:

$$Delay_{RED} = D_{RED} \times T_{TBCLK},$$
(2)

$$Delay_{FED} = D_{FED} \times T_{TBCLK},$$
(3)

where T_{TBCLK} is the period of time-based clock. Typical dead-time values should be in the range from 3 ms to 6 ms [18]. Considering that the clock of the DSP-TMS320F28335 is 150 MHz, T_{TBCLK} is equal to 6.66E-9. D_{RED} and D_{FED} are set to 500; therefore, $Delay_{RED}$ and $Delay_{FED}$ are equal to 3.33 µs.

The central processing unit clock for the DSP-TMS320F28335 is 150 MHz, and the switching frequency is 5 kHz. Therefore, the timer period value is equal to 30000. The output from the controller (V_{abc}) is in per unit amplitude. This value should increase up to 0.9 from the timer period value of 30000, where 0.9 is the maximum value for the modulation index. For calibration, the (V_{abc}) signals are multiplied by 27000, thus giving a value of 27000. Finally, six switching signals are obtained from the six pins of port 8. The signals are as follows: ePWMA1 for IGBT1 on pin 9, ePWMB1 for IGBT4 on pin 10, ePWMA2 for IGBT3 on pin 11,

ePWMB2 for IGBT6 on pin 12, ePWMA3 for IGBT5 on pin 13, and ePWMB3 for IGBT2 on pin 14. These six signals are fed to the gate driver circuits to increase the switching signal level to match with the IGBT gate level requirement. The real-time model shown in Fig. 2 is converted into C-code and automatically linked to the real-time DSP-TMS320F28335 processor using Code Composer Studio (CCS) software.
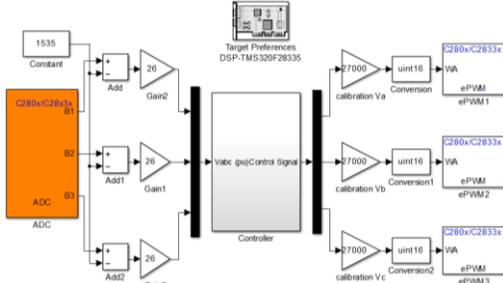

Fig.2. Real-time model of the SPWM via DSP-TMS320F28335 controller

5. Real-time implementation of the SVM

SVM is another type of the most important switching methods. SVM is implemented in the inverter controlling to extract sinusoidal AC waveforms from the VSI [21]. The real-time implementation of the SVM via a DSP-TMS320F28335 controller, which includes C280x/C28x3x ADC and C280x/C28x2833x ePWM, is shown in Fig. 3. Two ADC blocks are used; the first ADC block is used to read the V_{abc} voltage, and the second ADC block is used to read the V_{dc} voltage. The V_{abc} voltage is measured through pins 2, 3, and 4 from port 5 (ADCINB1, ADCINB2, and ADCINB3), whereas the V_{dc} voltage is measured through pin 2 from port 9 (ADCINA1). The bias should be experimentally removed from the ADC_{output} signal, which is achieved through subtracting from the half of the highest value. In the SVM, the bias is found to be 2056.
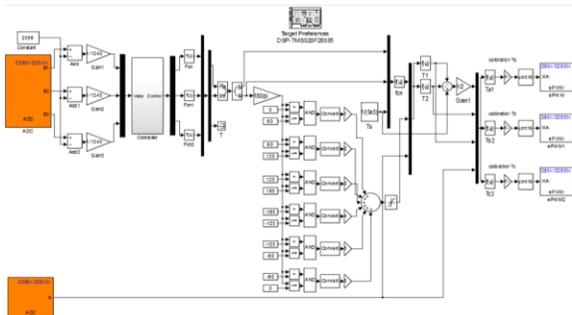

Fig.3. Real-time model of the SVM via DSP-TMS320F28335 controller

Three C280x/C28x2833x ePWM blocks are used in the implementation of the real-time model of the SVM via DSP-TMS320F28335 as can be shown in Fig. 3. Each ePWM block generates switching signals for one leg in VSI. Regarding to $Delay_{RED}$ and $Delay_{FED}$, the same delay used in SPWM is used in SVM which is 3.33 µs for fair comparison. As the switching frequency used is 5 kHz, the maximum amplitude for the (T_a, T_b and T_c) signals is 0.0002. This value should rise up to 0.9 from the timer period value of 30000, where 0.9 is the maximum value for the modulation index. For calibration, the (T_a, T_b and T_c) signals are multiplied by 135000000, thus giving a value of 27000. The six switching signals which are IGBT1, IGBT4, IGBT3, IGBT6, IGBT5, and IGBT2 will be on pins 9, 10, 11, 12, 13, and 14, respectively from Port 8. Finally, the gate driver circuits are used to increase the switching signals level to match with the IGBT gate level requirement. The real-time implementation of the SVM via DSP-TMS320F28335 is achieved using the model shown in Fig. 3 through CCS software.

6. Results and discussion

A 1.5 kW, 240 V, 50 Hz stand-alone PVS is used to test the proposed SVM for two-level voltage source inverter. Two types of loads have been used. The first load is *R* load with capacity 1.5 kW; whereas the second load is *RL* load which is implemented using a three phase induction motor with a capacity of 1.4 A, 50 Hz, 1405 rpm, and 1 HP.

The real-time model is down-loaded to DSP-TMS320F28335 via the CCS. The two-level VSI is controlled through the SVM switching signals generated from the DSP-TMS320F28335.

The experimental result for the VSI based SPWM is shown in Fig. 4. The output waveforms demonstrate stable waveforms with approximately peak value of 339 V and rms voltage of 240 V. Furthermore, the voltage signals are purely sinusoidal with 50 Hz which demonstrate a 120° phase shift.

However, the quality of the waveforms is shown through the total harmonic distortion (THD). The THD is inversely proportional with quality of the output waveform. Regarding to the THD rate, the goal is always to generate waveforms with lowest THD rate. Nevertheless, the VSI output waveforms are considered certified if the THD rate is less than 5% which comply with the IEEE Std 929-2000 international standard [14]. The THD rate for the VSI based SPWM is shown in Fig. 5. The THD rate is found to be 2.2% which is meeting with IEEE Std 929-2000 international standard.

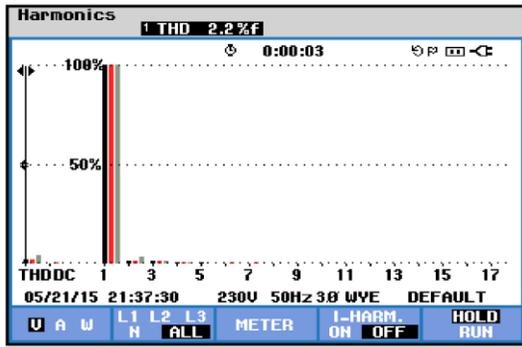**Fig. 4.** Output voltage waveforms based SPWM with *R* load

Fig. 5. THD spectrum based SPWM with *R* load

Fig. 6 shows the experimental result for the VSI based SVM. The output voltage waveform shows a constant peak with approximately of 339 V and 50 Hz sinusoidal output voltage waveforms with 120° displacement between the phases.

The THD rate for the VSI output voltage waveforms is shown in Fig. 7. The THD value for the voltage waveforms has been kept with a small percentage of 2.0% which is complying with the IEEE Std 929-2000 international standard. The low THD shows high quality output waveforms.
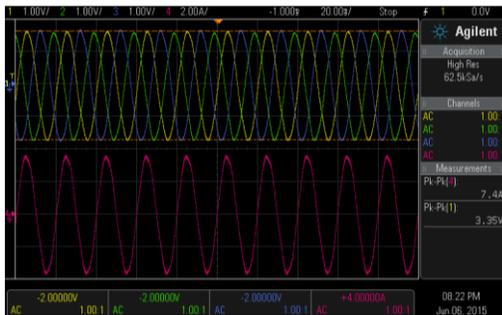

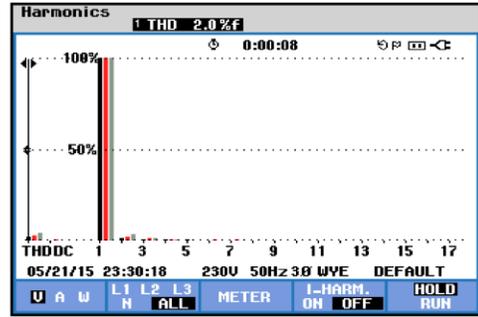**Fig. 6.** Output voltage waveforms based SVM with *R* load

Fig. 7. THD spectrum based SVM with *R* load

The second type of load is *RL* load. The *RL* load is implemented using motor with a capacity of 1.4 A, 50 Hz, 1405 rpm, and 1 HP. The output waveforms with the *RL* load based SPWM is shown in Fig. 8. The output voltage waveforms are kept with an approximately amplitude of 339 V. Moreover, the phase shift between each two phases is 120° and the frequency is 50 Hz.

The THD for the VSI output waveforms based SPWM with *RL* load is also calculate to verify with quality waveforms. The THD rate for voltage output waveforms is depicted in Fig. 9. It shows that the THD rate is found to be 3.1% which comply with the harmonic limit of 5% as specified in the IEEE Std 929-2000.
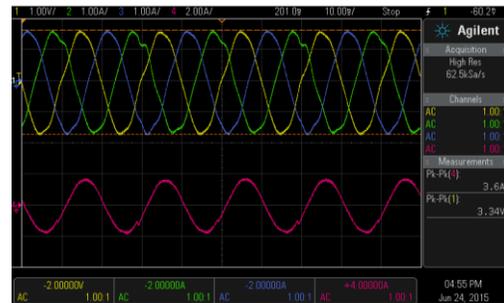

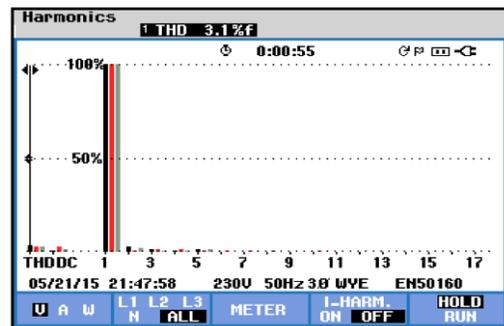**Fig. 8.** Output voltage waveforms based SPWM with *RL* load

Fig. 9. THD spectrum based SPWM with *RL* load

Fig. 10 shows the output voltage waveforms for the VSI based SVM with *RL* load. The figure clearly shows that the output waveforms are stable, and very clean without any negative effect. Furthermore, the amplitude is constant and has been kept with approximately amplitude of 339 V. Moreover, a 50 Hz of frequency is achieved with phase shift of 120°. This shows that the *RL* load can efficiently handle by SVM.

To verify the quality of the voltage signals for VSI, the THD is calculated as depicted in Fig. 11. High quality output voltage waveforms have been achieved where the THD rate is calculated to be 2.6%. The low percentage of the THD is fulfilling with IEEE Std 929-2000 international standard. This indicates that the SVM is sufficiently robust to achieve a favorable waveform with an *RL* load.
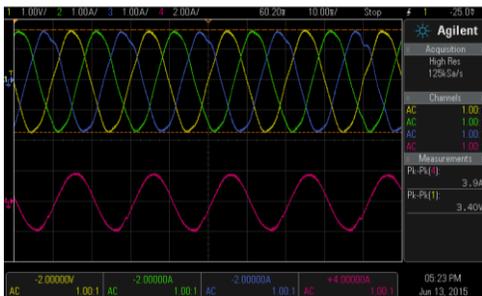

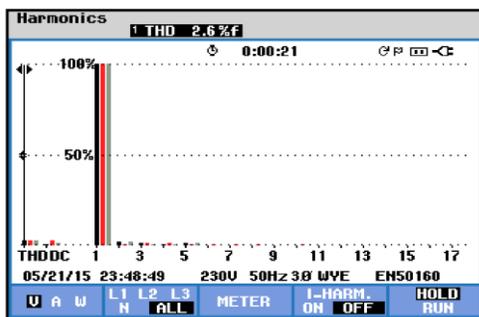**Fig. 10.** Output voltage waveforms based SVM with *RL* load

Fig. 11. THD spectrum based SVM with *RL* load

Table 1 shows the comparison results between the SVM and SPWM regarding to THD percentages. The table shows that the SVM achieved lowest harmonic of the output waveforms compared with SPWM. The limit of the harmonic indicates that the SVM is efficient and robust to deal with many types of loads such as *R* and *RL* loads. Accordingly, the SVM produces high quality waveforms with lowest THD which in turn leads to significantly enhance the performance of the overall system.

Table 1. THD comparison of SPWM and SVM

Type of load	SPWM	SVM
R load	2.2%	2.0%
RL load	3.1%	2.6%

7. Conclusion

The experimental investigation of SVM switching controller based two-level voltage source inverter for photovoltaic system using DSP-TMS320F28335 has been presented in this paper. The selection of the SVM can provide proper switching technique. The configuration of the controller based SVM has been implemented using DSP-TMS320F28335 control board. To validate the performance of the system, a prototype of the two-level VSI has been developed. Two types of loads have been used which are *R* and *RL* loads. The THD rates have been calculated to evaluate the VSI performance. The performance of the VSI based SVM has been compared with the performance of the VSI based SPWM. The hardware results reveal that the output voltage waveforms based SVM have been much enhanced where the THD values have been found to be 2.0% and 2.6% with *R* and *RL* loads, respectively; whereas the THD rates based SPWM have been found to be 2.2% and 3.1% with *R* and *RL* loads, respectively. Furthermore, the results show that the use of DSP-TMS320F28335 control board provides very high speed controller which lead to significantly improve the performance of the overall system.

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